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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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*Ex parte* JEFFERY F. HARNESS and DEAN WARREN

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Appeal 2009-000355
Application 09/750,090
Technology Center 2100

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Decided: June 24, 2010

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Before JOHN A. JEFFERY, ST. JOHN COURTENAY III, and STEPHEN C. SIU, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1, 7-10, and 19. Claims 2-6, 11-18, and 20-25 are allowed. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

*Invention*

The invention relates to filtering over-sampled serial data (Spec. 1, l. 3). The filtering includes detection logic to detect a sample bit having one logic value and, on either side of it, bits having the opposite logic value (Spec. 6, ll. 10-13; figs. 2a-b, 4).

Independent claim 10 is illustrative:

> 10. Apparatus for filtering over-sampled data comprising:
>
> a. detection logic coupled to receive a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits and to detect a sample bit having one logic value and adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit; and
>
> b. an output circuit outputting the received word with the sample bit having said one logic value inverted.

*Reference*

The Examiner relies upon the following reference as evidence in support of the rejection:

| | | |
|---|---|---|
| Obinata | US 5,034,744 | Jul. 23, 1991 |

*Rejection*

Claims 1, 7, 10, and 19 are rejected under 35 U.S.C. § 102(b) as being anticipated by Obinata.

Claims 8 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Obinata.

## ISSUE

The Examiner finds that "Obinata's objective is to remove/suppress the glitches in the input data . . . with positive glitches occur[ring] at '1' to '0' and negative glitches occur[ing] at '0' to '1'" (Ans. 7).

Appellants submit that Obinata's "'status change' is the situation where a previously sampled bit is different from a current sampled bit" (App. Br. 6).

*Issue*: Did the Examiner err in finding that Obinata teaches detecting a sample bit having one logic value and adjacent bits on both sides of the sample bit each having an opposite logic value to the one logic value of the sample bit?

## FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

1. Obinata teaches that "[i]f the next data from the output terminals $O_1$ to $O_4$ of the serial/parallel converting circuit 23, i.e., statuses of bits MSB [most significant bit] to 4SB [fourth most significant bit] of the next data is changed with respect to the previous data, the corresponding E-OR [exclusive-or] gates 34 to 37 become 'H' in their output levels" (col. 4, ll. 52-57).
2. Obinata teaches that "where the bit 4SB changes from '0' to '1' are detected, an output of AND gate 40 becomes 'H' . . . . where the

bit 4SB changes from '1' to '0' are detected, an output of AND gate 41 becomes 'H'" (col. 5, ll. 31-35).

3. Obinata teaches that

output terminals $O_1$ to $O_4$ of the serial/parallel converting circuit 23 are connected to data terminals D of D-type flip-flops (hereinafter referred to D-FF) 30 to 33, respectively. A latch clock RCK of the clock control circuit 22 is supplied to clock terminals CK of D-FF's 30 to 33. Output terminals Q and data terminals D of D-FF's 30 to 33 are connected to exclusive OR (E-OR) gates 34 to 37, respectively.

(Col. 4, ll. 39-46; fig. 1).

4. Obinata teaches that

The outputs of AND gates 40 and 41 are connected to data terminals D of D-FF's 44 and 45, respectively. A latch clock RCK from the clock control circuit 22 is supplied to clock terminals CK of D-FF's 44 and 45. An output terminal Q of D-FF 44 and a latch enabling signal LE are connected to a NAND gate 46. An output terminal Q of D-FF 45 and the latch enabling signal LE are connected to an AND gate 47. Outputs of NAND gate 46 and AND gate 47 are connected to each other through resistors $R_{43}$ and $R_{44}$.

(Col. 5, ll. 35-45; fig. 1).

## PRINCIPLES OF LAW

### *Anticipation*

Anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

## ANALYSIS

Appellants argue that Obinata's detection logic is limited to detecting that two adjacent bits have opposite values. The Examiner argues that Obinata discloses the claimed detection logic.

Obinata teaches detecting when the statuses of each bit MSB to 4SB is changed with respect to the previous data (FF 1, 3). Obinata specifically teaches detecting a change in 4SB from 0 to 1 or from 1 to 0 (FF 2), which the Examiner cites in clarifying the rejection (Ans. 7). However, the claimed invention requires detecting the condition wherein a sample bit has the opposite logic value of the adjacent bits on both sides of the sample bit, where each of the adjacent bits have an opposite logic value to the sample bit. (Claim 1). Thus, to anticipate the claimed invention, Obinata would have to detect the changes 0 to 1 to 0 or the changes 1 to 0 to 1. This is not possible with Obinata's disclosed use of flip-flops 30 to 33 and exclusive gates 34 to 37 because, for each bit MSB to 4SB, only the output terminal Q and data terminal D of each flip-flop are used as inputs to the exclusive OR gate for detecting a change in that bit (FF 3).

The Examiner further finds that in Obinata, the "values of AND gates [40 and 41] are later used to enable an inverting means for removing/suppressing the glitch if both of AND gates are 'H'" (Ans. 7). The outputs of AND gates 40 and 41 are connected to the data terminal of flip-flops 44 and 45 respectively (FF 4). These outputs can reflect a change in bit 4SB (FF 2). The outputs of flip-flops 44 and 45 are connected to NAND gate 46 and AND gate 47 respectively (FF 4). The outputs of gates

46 and 47 are connected to each other through resistors $R_{43}$ and $R_{44}$ (*id.*). Because the outputs of flip-flops 44 and 45 are reflected in the outputs of gates 46 and 47, which are connected to each other through resistors, Obinata use of the values of AND gates 40 and 41 reflects a single change in 4SB (i.e., either from 0 to 1 or from 1 to 0). The Examiner does not show how Obinata's disclosed circuitry produces output based on two changes in 4SB, or in any other bit. Therefore, the Examiner errs in finding that Obinata detects multiple changes in a bit (i.e., from 0 to 1 to 0 or from 1 to 0 to 1). The Examiner further fails to show that such detection would have been obvious in light of the teachings and suggestions of Obinata.

For at least these reasons, and since independent claims 1 and 19 contain similar limitations, we conclude that the Examiner erred in rejecting independent claims 1, 10, and 19, and claims 7-9 which depend therefrom.

## CONCLUSIONS OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner erred in finding that Obinata teaches detecting a sample bit having one logic value and adjacent bits on both sides of the sample bit each having an opposite logic value to the one logic value of the sample bit.

## DECISION

We reverse the Examiner's decision rejecting claims 1, 7, 10, and 19 under 35 U.S.C. § 102(b).

We reverse the Examiner's decision rejecting claims 8 and 9 under 35 U.S.C. § 103(a).

REVERSED

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